Product Information

To:

Product Name: TEC104040000

Document Issue Date: 2016/06/27

Customer	
SIGNATURE _____ _____ _____ Please return 1 copy for your confirmation with your signature and comments.	SIGNATURE REVIEWED BY QA _____ PREPARED BY FAE _____

Revision	Date	Page	Old Description	New Description	Remark
00	2016/06/27	all	--	First issue.	

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1.0 General Descriptions

1.1 Introduction

The TEC104040000 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 10.4-inch diagonally measured active display area with XGA resolution (1,024 horizontal by 768 vertical pixels array).

1.2 Features

- 10.4" TFT-LCD Panel
- LED Backlight System
- Supported XGA Resolution
- Compatible with RoHS Standard

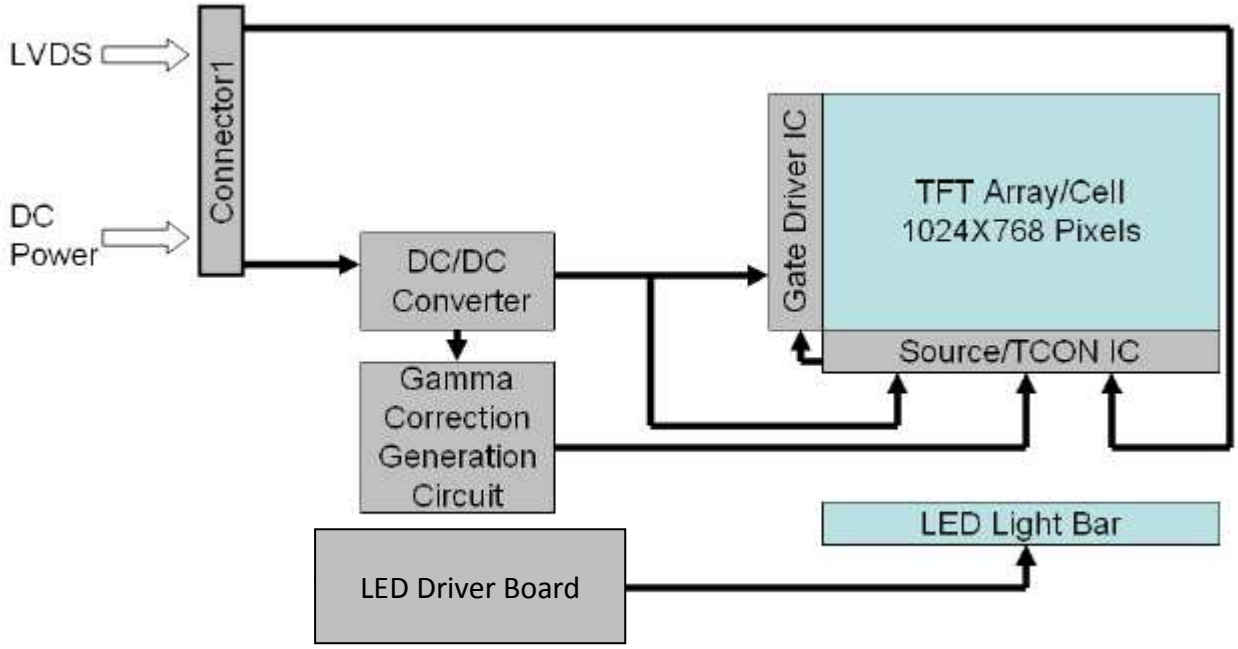
1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	10.4	inch
Active Area (H x V)	211.2 x 158.4	mm
Number of Pixels (H x V)	1,024 x 768	-
Pixel Pitch (H x V)	0.20625 x 0.20625	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White	-
White Luminance	(1600) (Typ)	cd /m^2
Contrast Ratio	(900) (Typ.)	-
Response Time	(16) (Typ.)	ms
Input Voltage	3.3 (Typ.)	V
Power Consumption	(8.8)(Max)	W
Weight	(340) (Max)	g
Outline Dimension (H x V x D)	(236.0) (Typ.) x 176.9(Typ.) x 7.85 (Typ.)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	262k/16.7M	-
Optimum Viewing Direction	6 o' clock	-
Surface Treatment	Anti-Glare	-

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram



2.0 Absolute Maximum Ratings

Table 1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	(-0.3)	(3.96)	V	(1)
Operating Temperature	TOP	-20	70	°C	(1) (2) (3) (4)
Operating Humidity	HOP	10	85	%RH	-
Storage Temperature	TST	-30	80	°C	-
Storage Humidity	HST	10	90	%RH	-

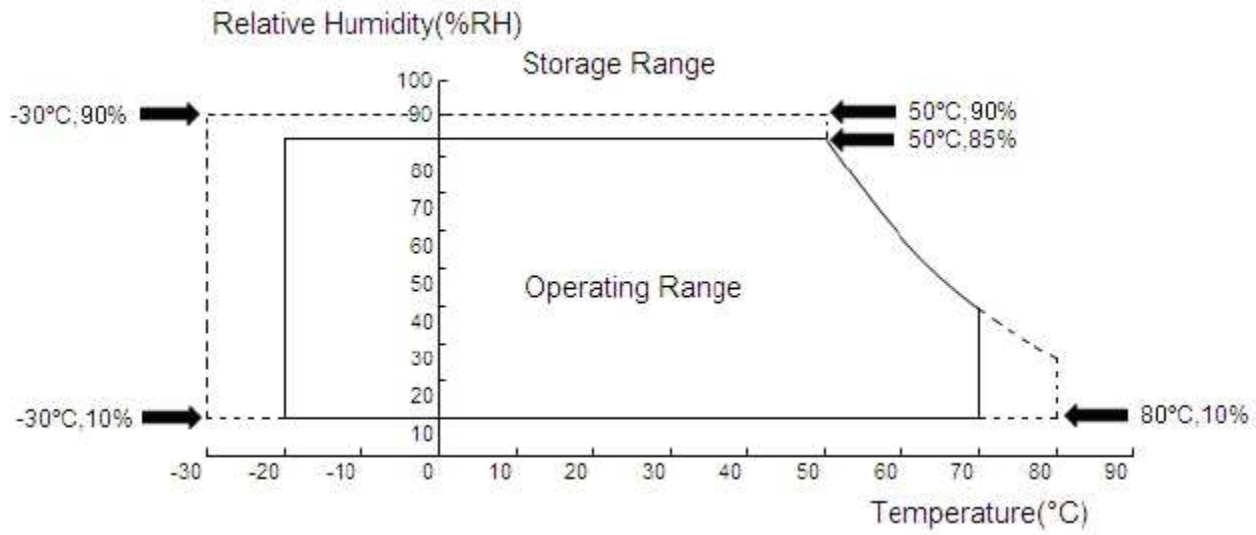
Note (1): Humidity: 85%RH Max. (T<=40°C) Note static electricity.
Maximum wet bulb temperature at 39°C or less. (T>40°C) No condensation.

Note (2): There is a possibility of causing deterioration in the irregularity and others of the screen and the display fineness though the liquid crystal module doesn't arrive at destruction when using it at 60~70°C or -20~0°C.

Note (3): There is a possibility of causing the fineness deterioration by the prolonged use in the (high temperature) humidity environment (60% or more).

Note (4): In the operating temperature item, the low temperature side is the ambient temperature regulations. The high temperature side is the panel surface temperature regulations.

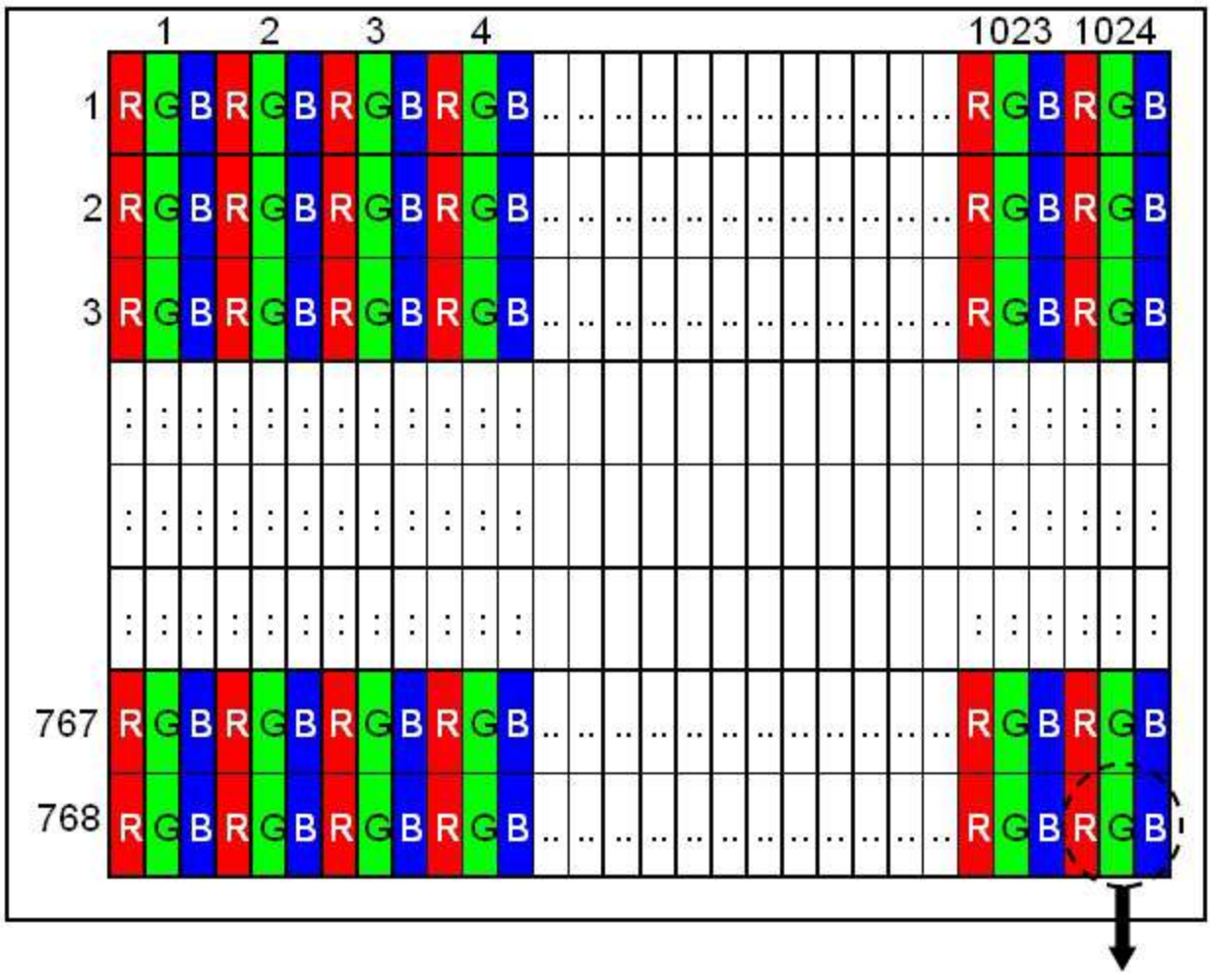
Figure 2 Absolute Ratings of Environment of the LCD Module



3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixel format image.

Figure 3 Pixel Format



4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

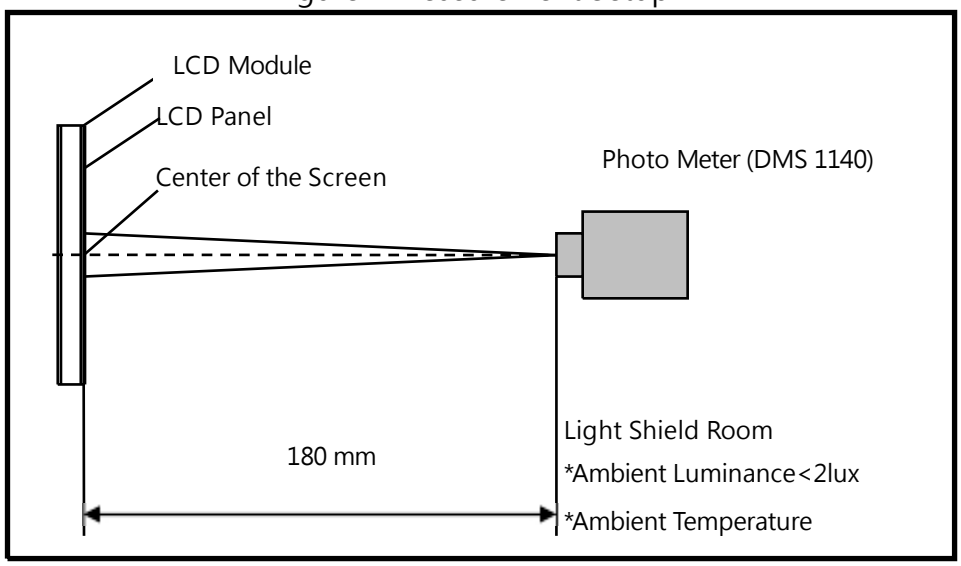
Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θ_{x+}	(70)	(75)	-	degree	(1),(2),(3)
		θ_{x-}	(70)	(75)	-		
	Vertical	θ_{y+}	(70)	(75)	-		
		θ_{y-}	(70)	(75)	-		
Contrast Ratio	Center		(720)	(900)	-	-	(1),(2),(4)
Response Time	Rising + Falling		-	(16)	TBD	ms	(1),(2),(5)
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	TBD	Typ. +0.03	-	(1),(2),(3) θx=θy=0°
	Red y			TBD		-	
	Green x			TBD		-	
	Green y			TBD		-	
	Blue x			TBD		-	
	Blue y			TBD		-	
	White x		(0.260)	(0.310)	(0.360)	-	
	White y		(0.280)	(0.330)	(0.380)	-	
NTSC	-		(48)	(50)	-	%	(1),(2),(3) θx=θy=0°
White Luminance	Center		(1500)	(1600)	-	cd/m^2	(1),(2),(6)
Luminance Uniformity	9 Points		(75)	(80)	-	%	(1),(2),(7)

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25°C) for 15 minutes to Avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a

Figure 4 Measurement Setup



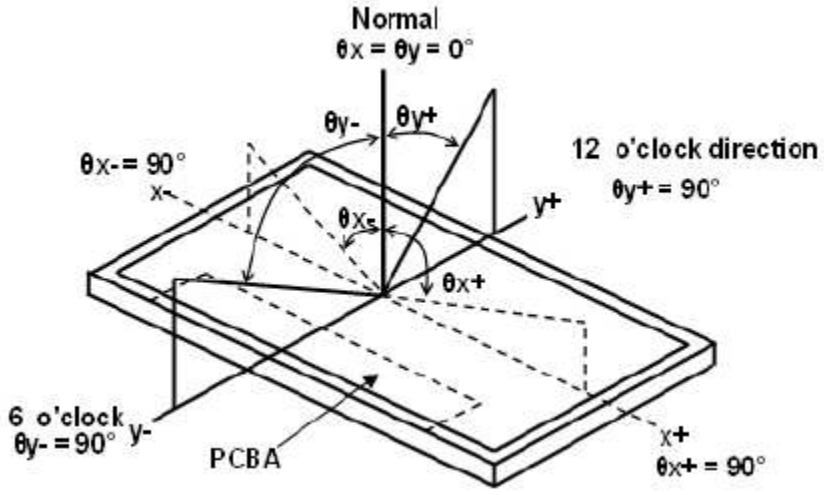
Note (2) The LED input parameter setting as:

V_LED: 12V (±0.1V)

PWM_LED: duty 100 %

Note (3) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (4) Definition Of Contrast Ratio (CR)

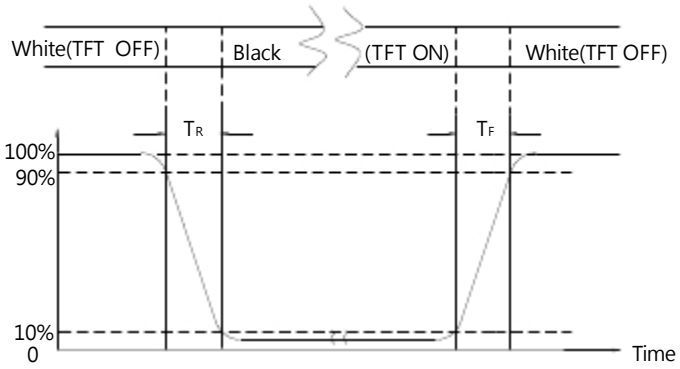
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (5) Definition Of Response Time (TR, TF)

Figure 6 Definition of Response Time



Note (6) Definition Of Luminance White

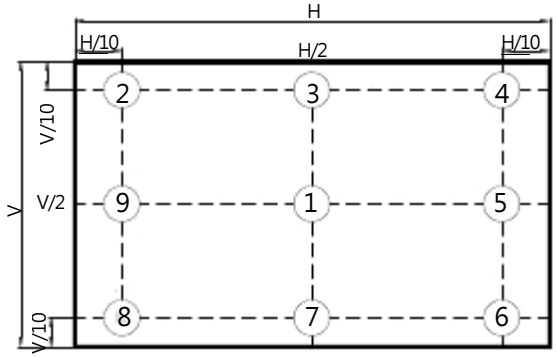
Measure the luminance of gray level 255 at center point (Ref.: Active Area)

Note (7) Definition Of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of gray level 255 at 9 points.

$$UNF(9pts) = \frac{Min(L1, L2, \cdots L9)}{Max(L1, L2, \cdots L9)}$$

Figure 8 Measurement Locations Of 9 Points



5.0 Backlight Characteristics

5.1 Parameter Guideline Of LED Backlight

Table 3 Parameter Guideline for LED Backlight

Symbol	Description	Min.	Typ.	Max.	Unit	Note
IR_{LB}	L/B String Current	-	260	-	[mA]	Operating with fixed driving current
V_{LB}	L/B String Voltage	-	-	30.6	[Volt]	
P_{BLU}	LED Light Bar Power Consumption	-	-	7.96	[Watt]	
LT_{LB}	L/B Life Time	30,000	-	-	[Hour]	

Note 1: Ta means ambient temperature of TFT-LCD module,

Note 2: If module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 3: Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

Table 4 Backlight Connector Type

Item	Description
Type	PHR-2
Mating Receptacle / Type (Reference)	SPH-002T-P0.5S

Table 5 Backlight Connector Pin Assignment

Pin No.	Symbol	Signal name
1	VCC	High Voltage
2	GND	Low Voltage

6.0 Electrical Characteristics

6.1 Interface Connector

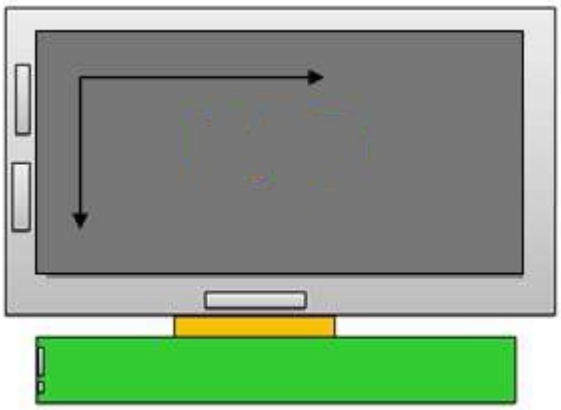
Table 6 Signal Connector Type

Item	Description
Type/Part Number	MSB24013P20HA (Manufacture by STM)
Mating Receptacle / Type (Reference)	P24013P20 or compatible

Table 7 Signal Connector Pin Assignment

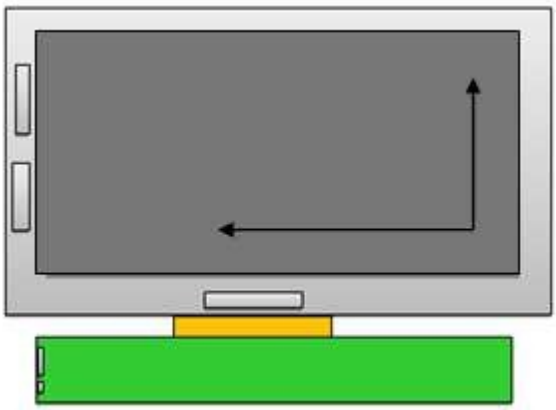
Pin No.	Symbol	Description	Note
1	VDD	Power Supply, 3.3V (typical)	-
2	VDD	Power Supply, 3.3V (typical)	-
3	VSS	Ground	-
4	REV	Reverse Scan selection {High:2.5(min), 3.3(typ),3.6(max); Low: 0.5(max)}	(1)
5	Rin1-	-LVDS differential data input (R0-R5,G0)	-
6	Rin1+	+LVDS differential data input (R0-R5,G0)	-
7	VSS	Ground	-
8	Rin2-	-LVDS differential data input (G1-G5,B0-B1)	-
9	Rin2+	+LVDS differential data input (G1-G5,B0-B1)	-
10	VSS	Ground	-
11	Rin3-	-LVDS differential data input (B2-B5,HS,VS,DE)	-
12	Rin3+	+LVDS differential data input (B2-B5,HS,VS,DE)	-
13	VSS	Ground	-
14	CIkIN-	-LVDS differential clock input	-
15	CIkIN+	+LVDS differential clock input	-
16	GND	Ground	-
17	Rin4-	-LVDS differential data input (R6-R7,G6-G7,B6-B7)	-
18	Rin4+	+VDS differential data input (R6-R7,G6-G7,B6-B7)	-
19	SEL68	6/8 bits LVDS data input selection(H:8bits L/NC:6bits)	-
20	Bist	Internal use	-

Note (1) REV = LOW/NC



REV = High

;



6.2 LVDS Receiver

6.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 8 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	V_{CM} =+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	V_{CM} =+1.2V
Magnitude Differential Input Voltage	$\|V_{ID}\|$	200	-	600	mV	-
Common Mode Voltage	V_{CM}	1.0	1.2	1.4	V	Vth – Vtl=200 mV
Common Mode Voltage Offset	V_{CM}	-50	-	+50	mV	Vth – Vtl=200 mV

Note: (1) Input signals shall be low or Hi- resistance state when VDD is off.

(2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Figure 10 Voltage Definitions

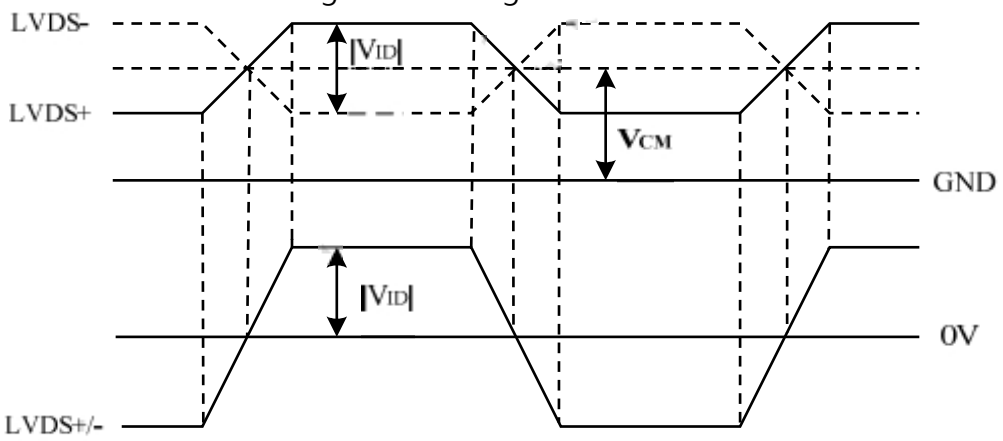


Figure 11 Measurement System

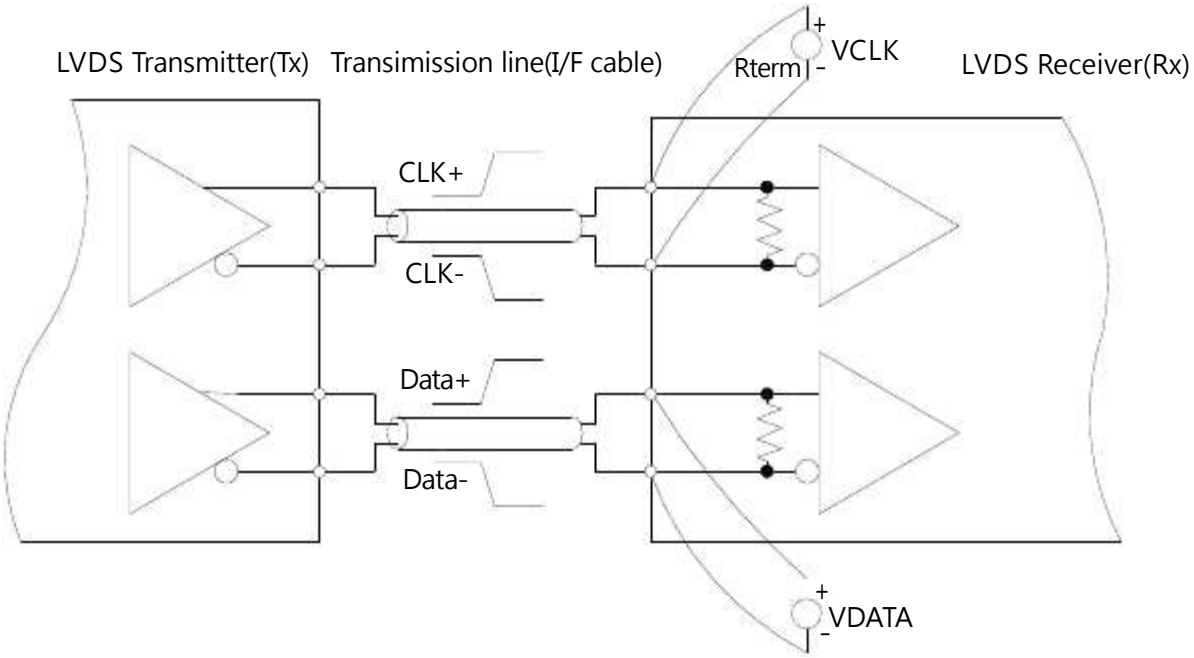


Figure 12 Data Mapping (6 Bit)

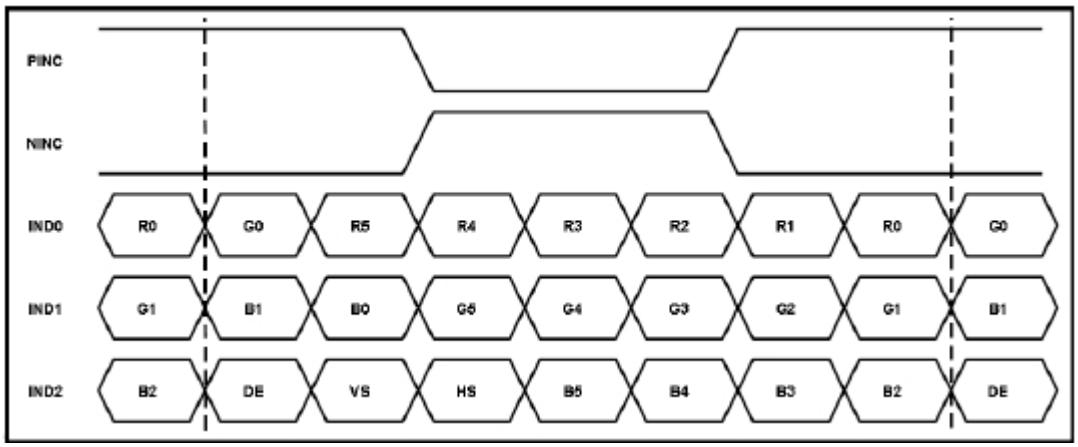
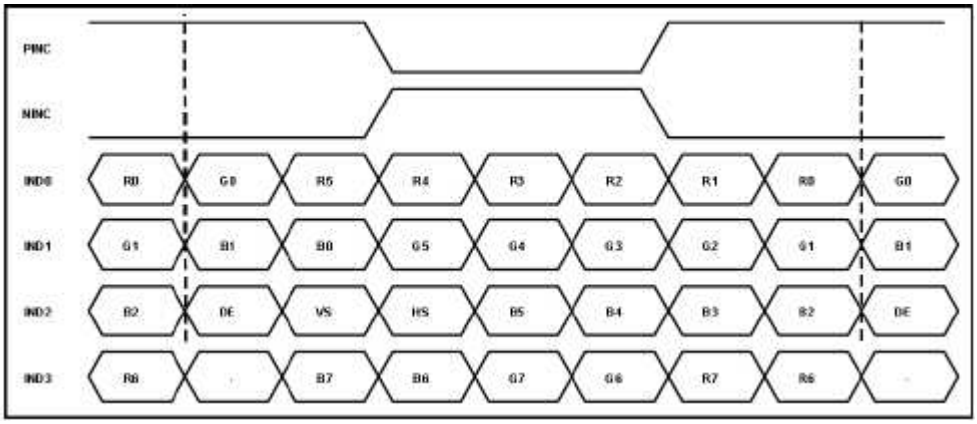


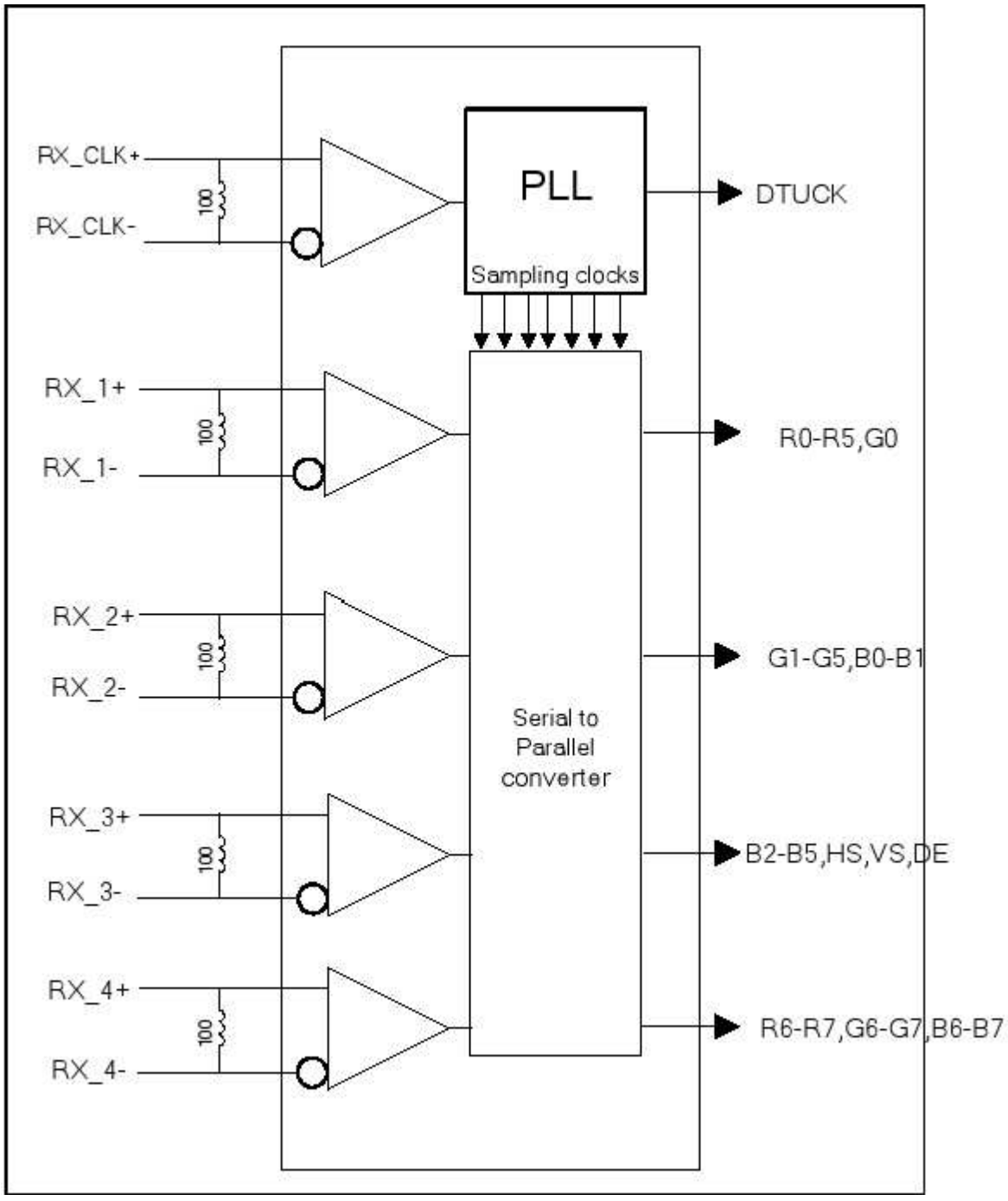
Figure 13 Data Mapping (8 Bit)



6.2.2 LVDS Receiver Internal Circuit

Figure 14 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 14 LVDS Receiver Internal Circuit



7.0 Interface Timings

7.1 Timing Characteristics

Synchronization method should be DE mode.

Table 9 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
LVDS Clock Frequency	Fclk	MHz	(52)	(65)	(71)
H Total Time	HT	Clocks	(1,114)	(1,344)	(1,400)
H Active Time	HA	Clocks	1,024	(1,024)	1,024
H Blanking Time	HBL	Clocks	90	320	376
V Total Time	VT	Lines	(778)	(806)	(845)
V Active Time	VA	Lines	768	768	768
V Blanking Time	VBL	Lines	(10)	(38)	(77)
Frame Rate	Vsync	Hz	55	60	65

Note: H Blanking Time and V Blanking Time can not be changed at every frame.

8.0 Power Consumption

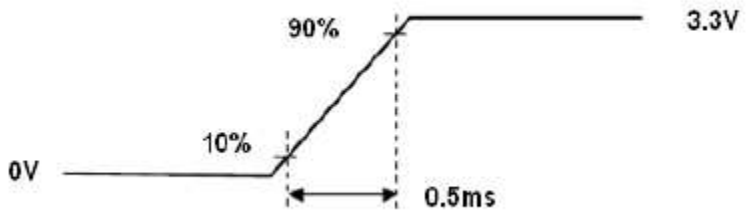
Input power specifications are as follows.

Table 10 Power Consumption

Item		Symbol	Min.	Typ.	Max.	Units	Note
LCD Drive Voltage (Logic)		VDD	3.0	3.3	3.6	V	(2), (4)
VDD Current	Black Pattern	IDD	-	TBD	(0.25)	A	(3),(4)
VDD Power Consumption	Black Pattern	PDD	-	-	(0.84)	W	
Rush Current		Irush	-	-	1.5	A	(1),(4)
Allowable Logic/LCD Drive Ripple Voltage		VDDrp	-	-	(200)	mV	(4)

Note (1) Measure Condition

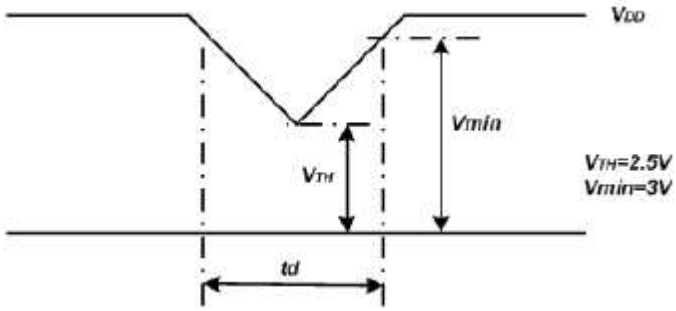
Figure 15 VDD Rising Time



Note (2) VDD Power Dip Condition

If VTH＜VDD≤Vmin，then td≤10ms；when the voltage return to normal our panel must revive automatically.

Figure 16 VDD Power Dip



Note (3) Frame Rate=60Hz, VDD=3.3V,DC Current.
Note (4) Operating temperature 25°C, humidity 55%RH.

9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD is off.

Figure 17 Power Sequence

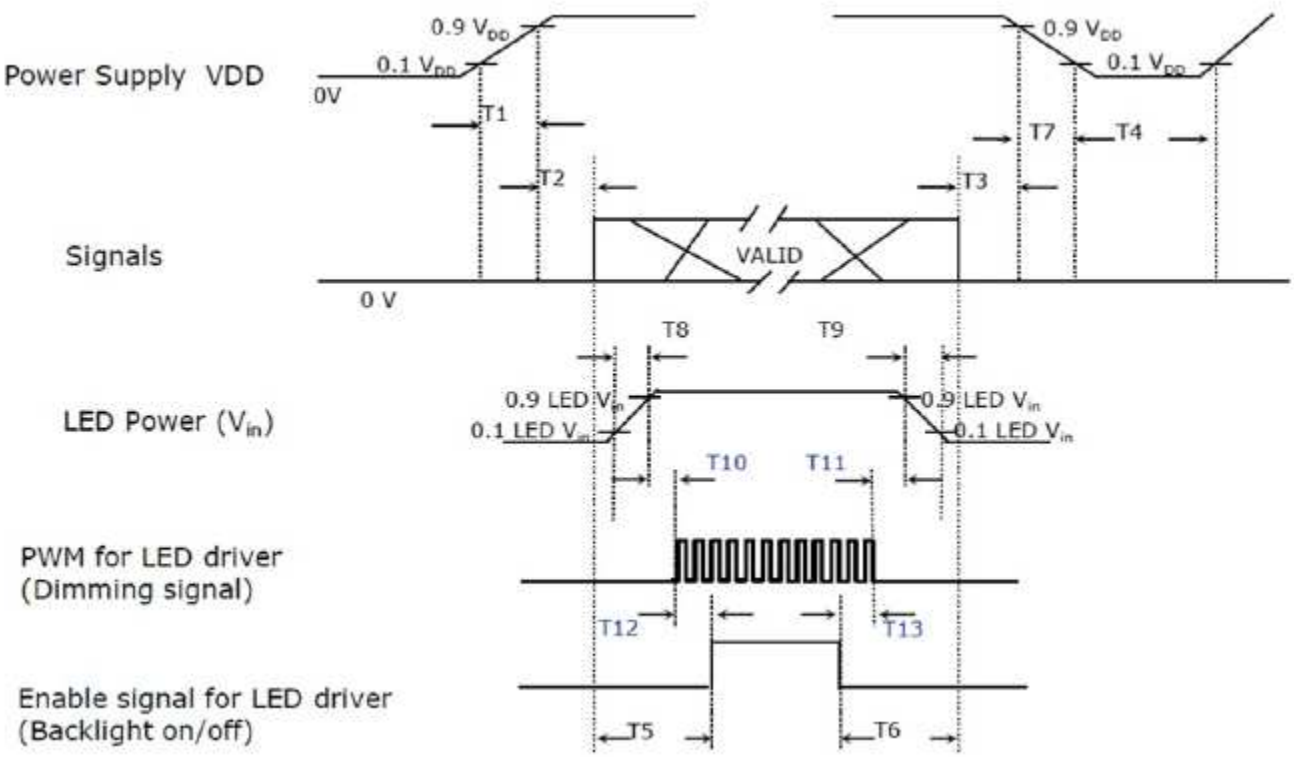


Table 10 Power Sequencing Requirements

Power ON/OFF Sequence					
Items	Symbol	MIN	TYP	MAX	Unit
VDD rising time from 10% to 90%	T1	0.5	-	10	ms
Delay from VDD to valid data at power ON	T2	30	-	50	ms
Delay from valid data OFF to VDD OFF at power OFF	T3	0	-	50	ms
VDD OFF time for windows restart	T4	500	-	-	ms
Delay from valid data to B/L enable at power ON	T5	200	-	-	ms
Delay from valid data off to B/L disable at power Off	T6	200	-	-	ms
VDD falling time from 90% to 10%	T7	0.5	-	10	ms
LED Vin rising time from 10% to 90%	T8	0.5	-	10	ms
LED Vin falling time from 90% to 10%	T9	0.5	-	10	ms
Delay from LED driver Vin rising time 90% to PWM ON	T10	0	-	-	ms
Delay from PWM Off to LED driver Vin falling time 10%,Must keep rule	T11	0	-	-	ms
Delay from PWM ON to B/L Enable ON,Must keep rule	T12	0	-	-	ms
Delay from B/LEnable Off to PWM Off	T13	0	-	-	ms

10.0 Mechanical Characteristics

10.1 Outline Drawing

Figure 18 Reference Outline Drawing (Front Side)

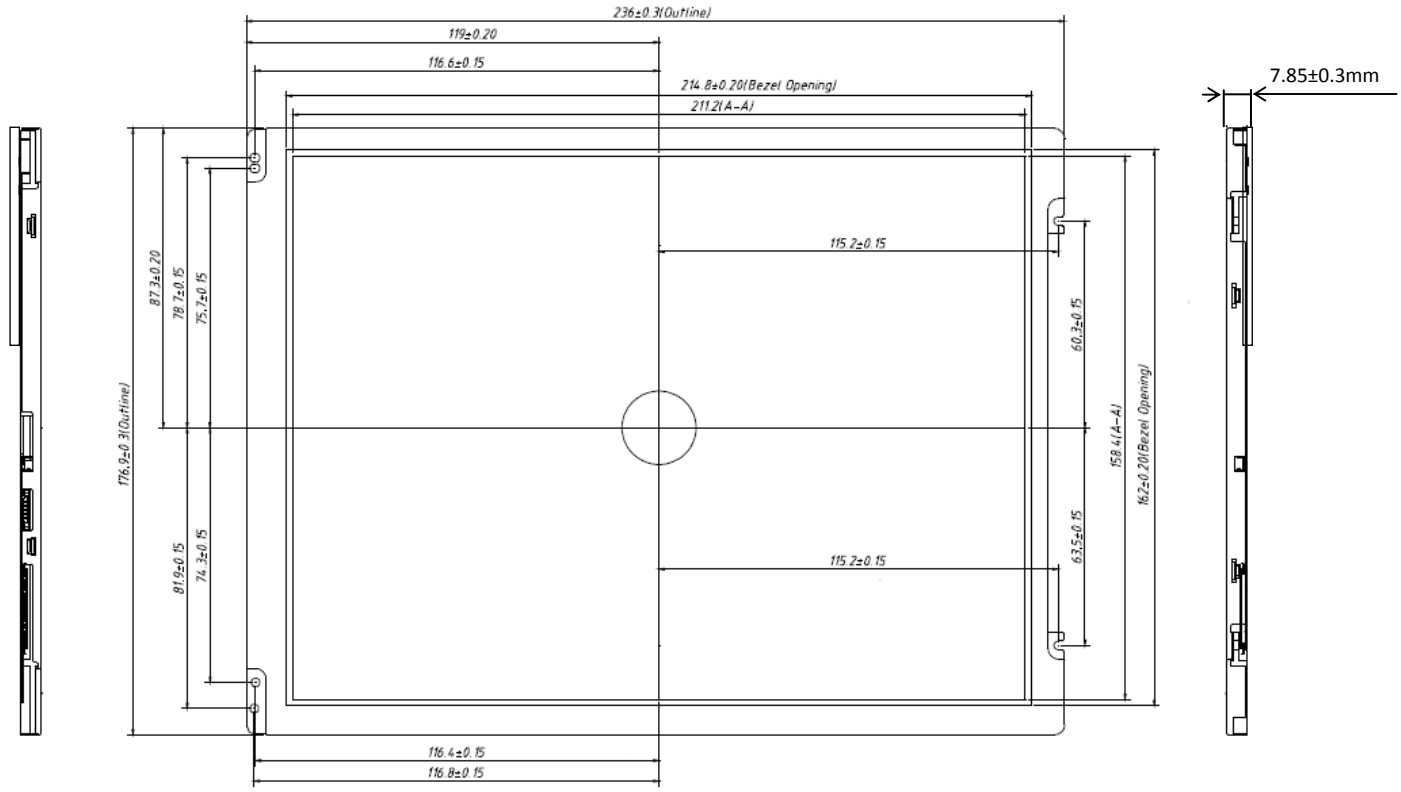


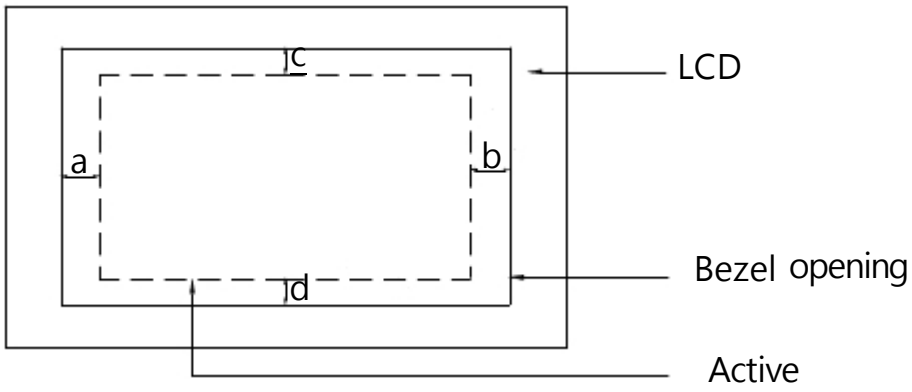
Figure 19 Reference Outline Drawing (Back Side)

10.2 Dimension Specifications

Table 11 Module Dimension Specifications

Item	Min.	Typ.	Max.	Units
Width	(235.7)	(236.0)	(236.3)	mm
Height	(176.6)	(176.9)	(177.2)	mm
Thickness	(7.5)	(7.85)	(8.15)	mm
Weight	-	-	(340)	g
BM：|a-b| & |c-d|	≤1.0			mm

Figure 20 BM Area



11.0 Reliability Conditions

Item		Package	Test Conditions		Note
High Temperature Operation Test		Module	70°C , 240hrs		1,4,5,6,7,8
Low Temperature Operating Test		Module	-20°C , 240hrs		1,4,5,6,7,8
High Temp./High Humidity Operating Test		Module	50°C , 85%, 240hrs		1,4,5,6,7,8
High Temp./High Humidity Storage Test		Module	50°C , 90%, 240hrs		1,5,6,7,8
Thermal Shock Non-operation Test		Module	-30°C ~80°C ,1hr/each cycle, 100cycles		1,5,6,7,8
Shock		Module	3 shock in each direction Peak acceleration:981m/s2 Half Sine Wave; 6ms		1,7,8
Vibration		Module	1.5G , 10~500 Hz , x、y、z each axis/1h		1,7,8
Drop Test		With package	(65)cm, 1corner,3 arris,6 side		1,8
Vibration Test		With package	1.5G , 10~500 Hz , x、y、z each axis/1h		1,8
ESD Test	operating	Module	contact	± 8 KV	2,4,5,7,8
			air	± 15 KV	
	non-operating		contact	± 10 KV	
			air	± 20 KV	
Image Sticking test		Module	5*7 chessboard pattern: 1. Normal temperature(25°C) :50% Grayscale,2h/10s,4h/10s,8h/2min,24h/5min ND8% OK 2. High temperature(70°C) :50% Grayscale ,2h/10s,4h/10s,8h/2min,24h/10min ND8% OK		3,4,6,7,8

Note:

1. There is no function defect and occurrence of any new defective shall not be allowed.
2. In case of malfunction defect caused by ESD damage. If it would be recovered to normal state after resetting, it would be judge as pass.
3. 25℃: Image Sticking is not visible through 8% ND filter after 5 min with pattern L127.
   70℃: Image Sticking is not visible through 8% ND filter after 10 min with pattern L127.
4. In Operating test, the B/L voltage and current must be in spec.
5. All the judgments are under normal temperature and the sample need to be static more than 2 hours in the normal temperature before judge.
6. During measurement, the condensation water or remains shall not be allowed.
7. The minimum sample quantity of test is 3pcs.
8. There is no display function fail issue occurred, all the cosmetic specification is judged before the reliability stress.